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MS-7851

ITX
Ver: 2.2

Intel Sharkbay plamform H81

CPU:

INTEL-Haswell LGA1150

System Chipset:

INTEL-LYNX

Memory:

DDRIII (1333/1666MHz) * 2 (Dual Channel)

PWM:

VRD12 - ISL95812

OnBoard Chipset:

HD Audio Codec:RTL887

LAN-realtek8111G

SIO:NUVOTON 5533D

SPI ROM: 64 MB

Expansion Slots:

PCI Express (X16) Slot * 1

Other:

DVI*1/HDMI*1

VGA*1

SATA2*2

SATA3*2

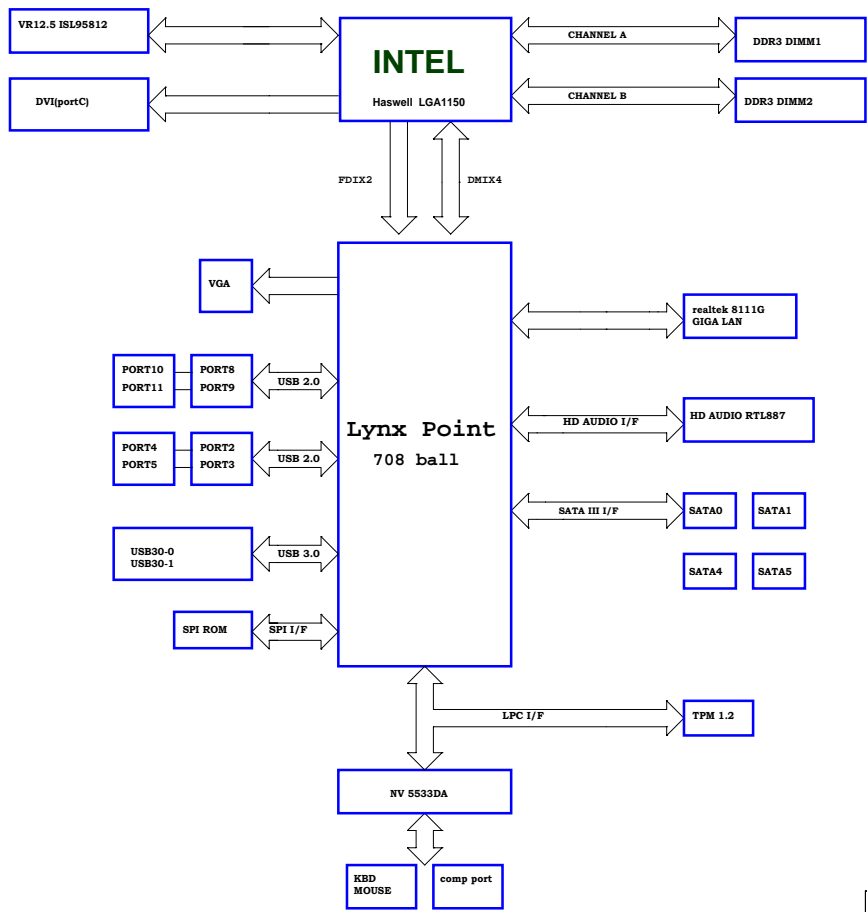
FRONT USB2.0 *4

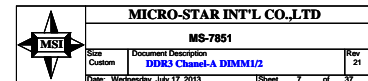
REAL USB2.0 *2

REAL USB3.0 *2

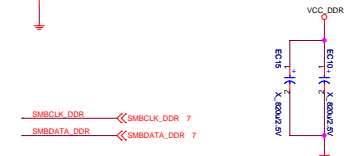
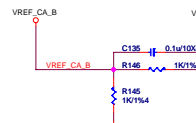
FRONT USB3.0 *2

MS-7851-2.2 Block Diagram





VCC_DDR VCC3_SPD VTT_DDR



DDR3

DDRIII-240P BLACK-RH-33



MS-7851

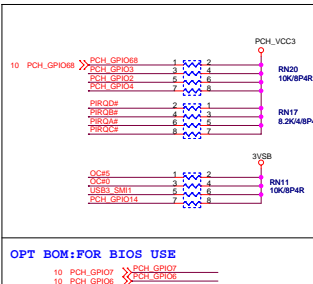
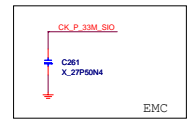
Size	Document Description
Custom	DDR3 Chanel-B DIMM3/4

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19 NEC_USB_TX      <==
19 NEC_USB_TX#     <==
18 PE3_LAN_TX      <==
18 PE3_LAN_TX#     <==

```

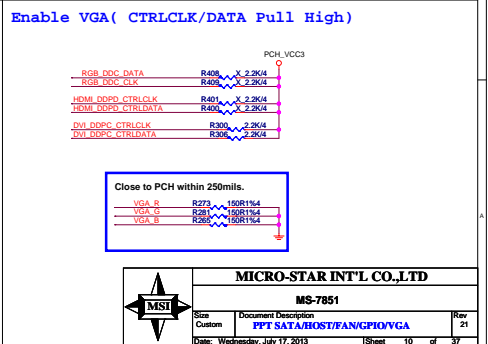
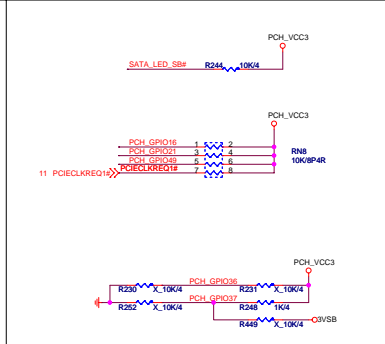
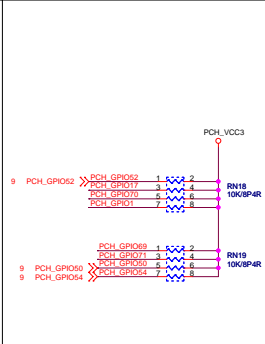
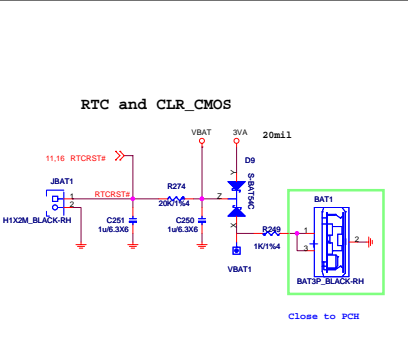


CLK96M_DOT_N	3	4
CK_14P8M_PCH	5	6
	7	8
CLKIN_GND0_N	R412	10K/4
CLKIN_GND0_P	R413	10K/4
CLK100M_DM1_N	R414	10K/4
CLK100M_DM1_P	R415	10K/4

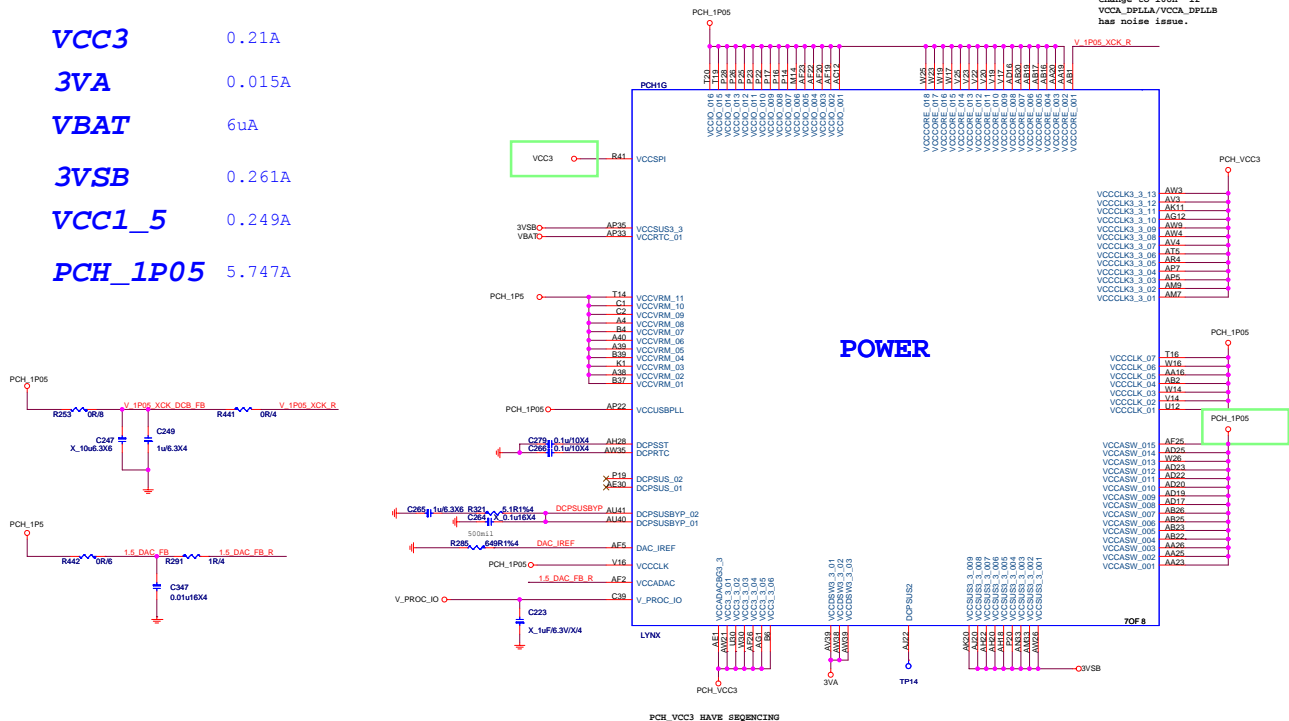


Size Custom	Document Description PPT PCIE/DMI/USB/CLK	Rev 2
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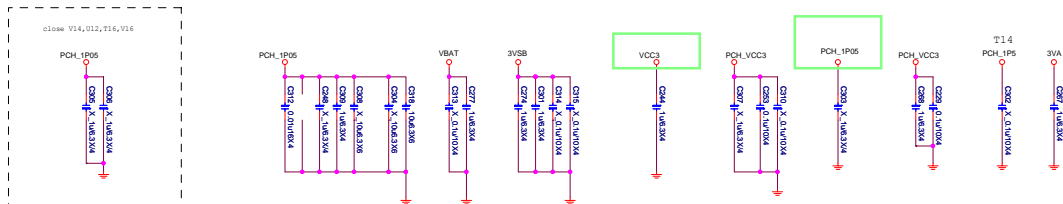
5,11,14,16 CHIP_PWGD >>> R296 0R1A ME_PWGD



VCC3 0.21A
3VA 0.015A
VBAT 6uA
3VSB 0.261A
VCC1_5 0.249A
PCH_1P05 5.747A

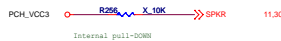


PCH decoupling cap



MICRO-STAR INT'L CO., LTD		
MS-7851		
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Custom	LYNX-POWER PIN	21
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PCH Straps



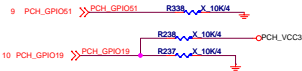
SPKR

Default Mode:
Internal weak Pull-down.
No Reboot Mode with TCO Disabled:
Connect to Voc3.3 with 8.2k-10k Ohm weak pullup resistor.



GPIO55

Default Mode:
Internal pull-up.
Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.



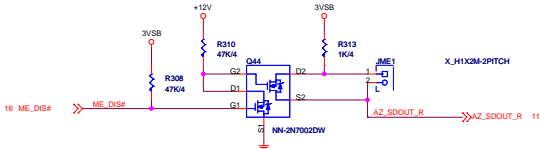
SATA1GP/GPIO19, GPIO51

Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.
Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.
Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.



GPIO53

Do not pull low.
Connect to ground with 1k Ohm pull-down resistor.



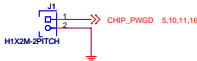
HDA_SDO

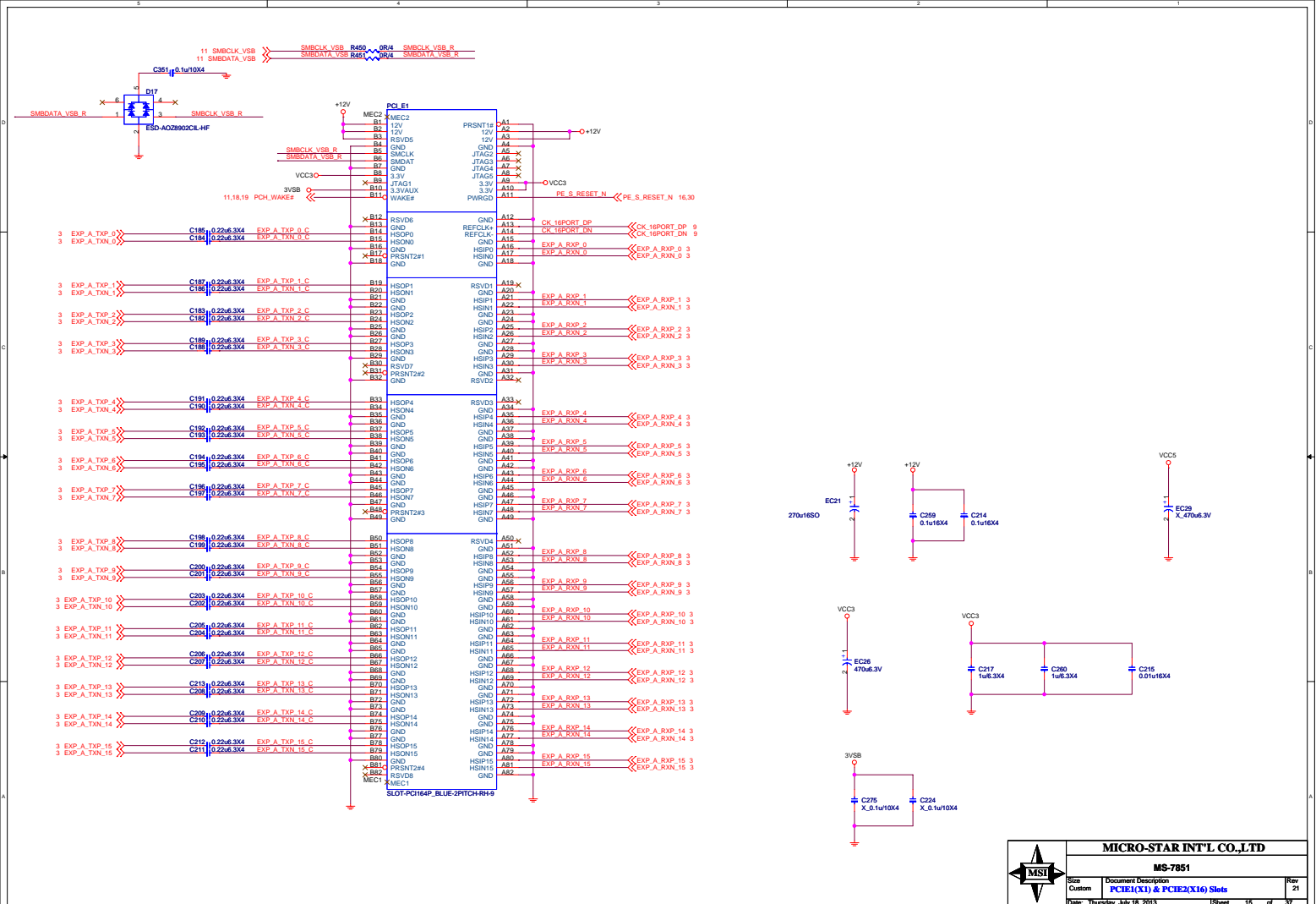
Default:
Do not pull high.
Disable ME in Manufacturing Mode:
Connect to VccSusDA with 1k Ohm pull-up resistor through a jumper.

GPIO37

Enable TLS:
Pull up with 1k Ohm to VccSus3.3.
Default (Disable TLS):
Leave NC. Internal pull down.

For test cpu voltage





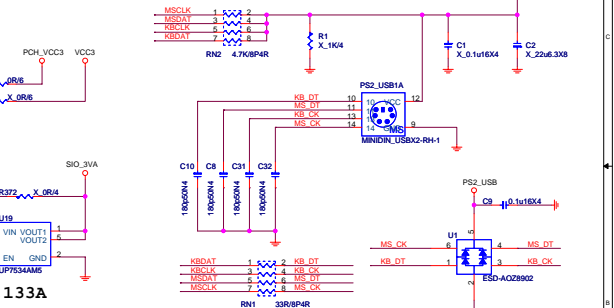
MICRO-STAR INT'L CO.,LTD

MS-7851

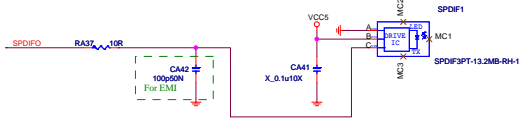
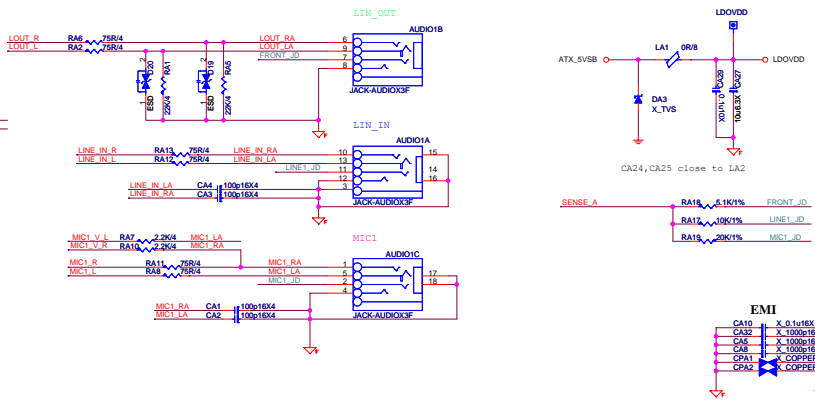
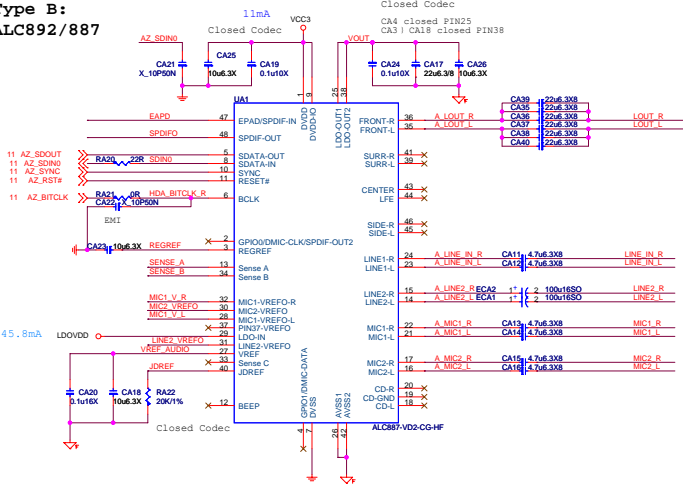
Size	Document Description
Custom	PCIE1(X1) & PCIE2(X16) Slots

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Date: Thursday, July 18, 2013 Sheet 15 of 37

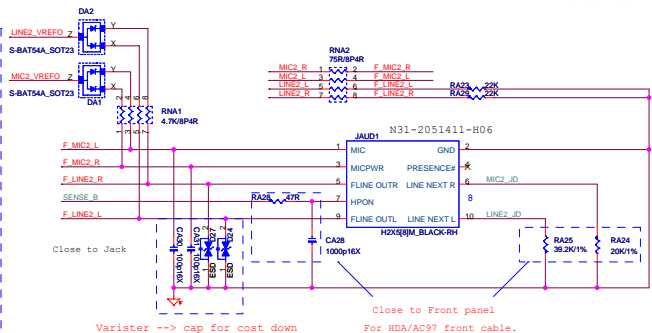
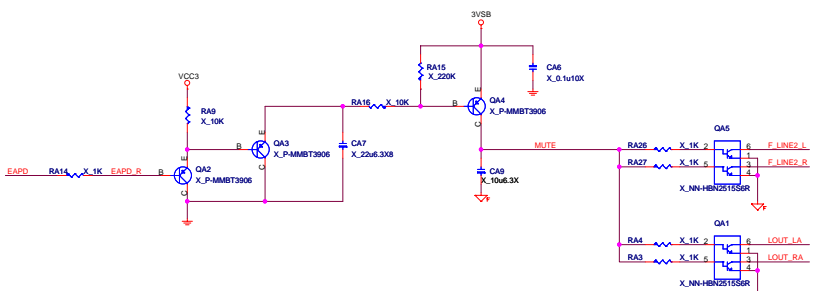


Type B:
ALC892/887



Rear Line OUT De-POP circuit

(add de-pop circuit by PM spec or customer request)



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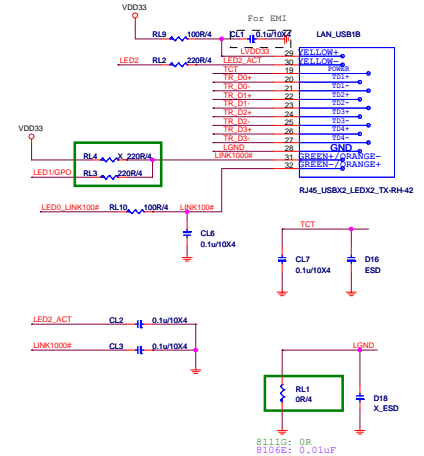
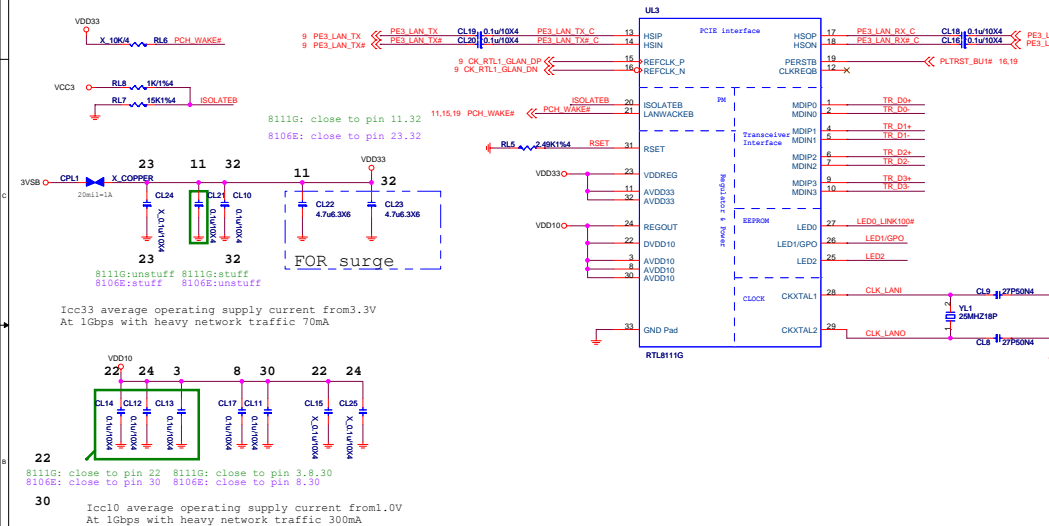
150 3051

Size Custom	Document Description Audio Codec ALC892/887	Rev 21
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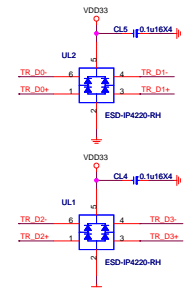
RTL8111G Giga LAN

RTL8106E 10/100M LAN

LAN Connector

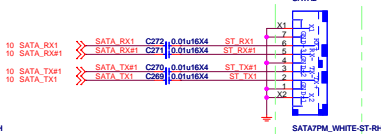


Reserve ESD Protect

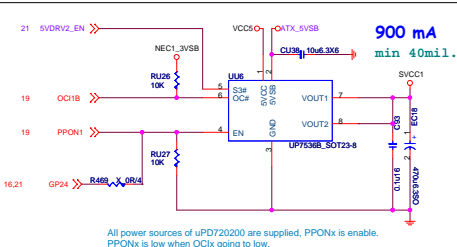
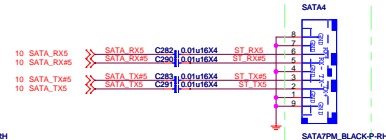
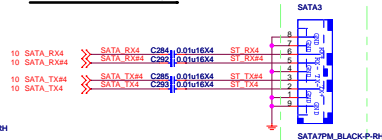


	MICRO-STAR INT'L CO.,LTD			
	MS-7851			
	Size	Document Description	Rev	
	Custom	LAN RTL8111G/8106E	21	
Date: Wednesday, July 17, 2013		Sheet	18	of 37

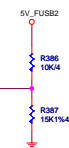
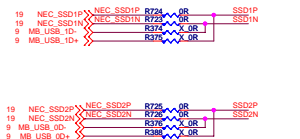
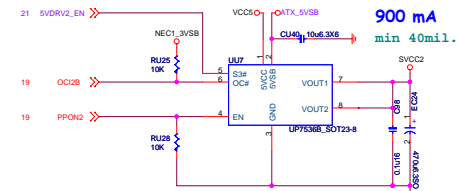
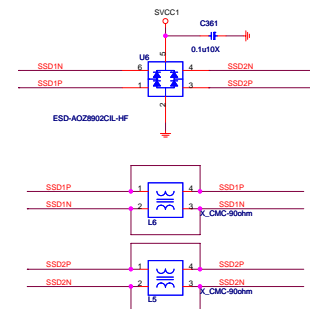
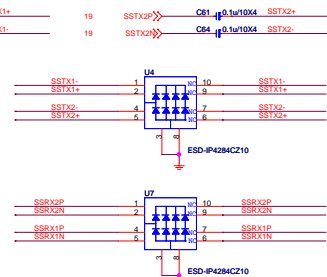
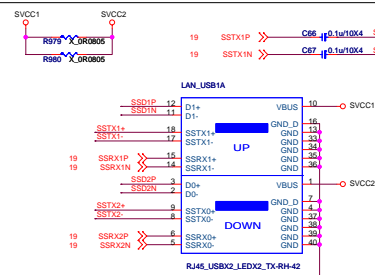
SATA 6G PORT 0,1



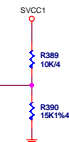
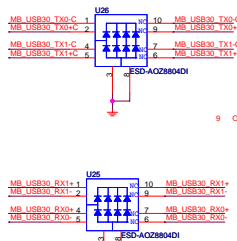
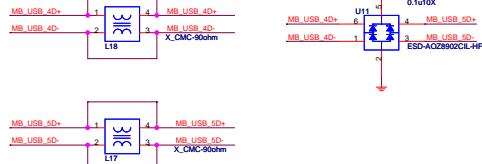
SATA 3G PORT 4,5



All power sources of uPD720200 are supplied, PPONx is enable.
PPONx is low when OC1x going to low.



Front USB 3.0



5V DIMM FOR USB

VCC5 = R461 510K/4
25.30 ATX_PWR_OK >> R462 10K/1%4 5VUSB 5V
11.16,25,29 SLP_S3+ >> U27 S3+ 56
11.16,19,25,28 SLP_S4+ >> U28 S4+ 56
16.20 GP24 >> MODE uP7501
5VUSB 5VSB C147 0.1uF104
R463 10K/4 ATX_5VSB
5VUSB DRV 7
5VSB DRV2 R98 OR
5VSB DRV2 F
C257 X 0.1uF10X
C258 X 10uF16X
Q109 P-P06P03
G
VCC5
R465 OR
5V DRV2
R466 OR
5V DRV2 F
C357 X 0.1uF10X
Q110 N-FAK53J0DPA-000JSA
VCC5
+12V
7501 Mode
B:Support 60/53/55
L:Support 60/53

USB MODE

20 5V DRV2_EN << 5V DRV2_EN
5V DRV2 R733 200K/1%4
5V DRV2 EN
VCC5 ATX_5VSB
C24 10uF 3V0603
5V USB
U22 S3+ 56
5V USB
VOUT1 7
VOUT2 8
EN
UP7536BMA8
16 PS2_MODE >>
R734 56K/1%4
PS2_USB
C92 22uF 3V06

FRONT USB PORT 10,11

9 MB_USB_11D >> L15 MB_USB_11D-
9 MB_USB_11D+ >> MB_USB_11D+
X CMC-90ohm
9 MB_USB_10D >> L16 MB_USB_10D-
9 MB_USB_10D+ >> MB_USB_10D+
X CMC-90ohm
5V_FUSB1
C359 0.1uF10X
MB_USB_10D- 6
MB_USB_11D+ 3
MB_USB_10D+ 1
MB_USB_11D- 4
NEAR CONNECTOR
H2X59JM_BLACK-RH-3

FRONT USB PORT 8,9

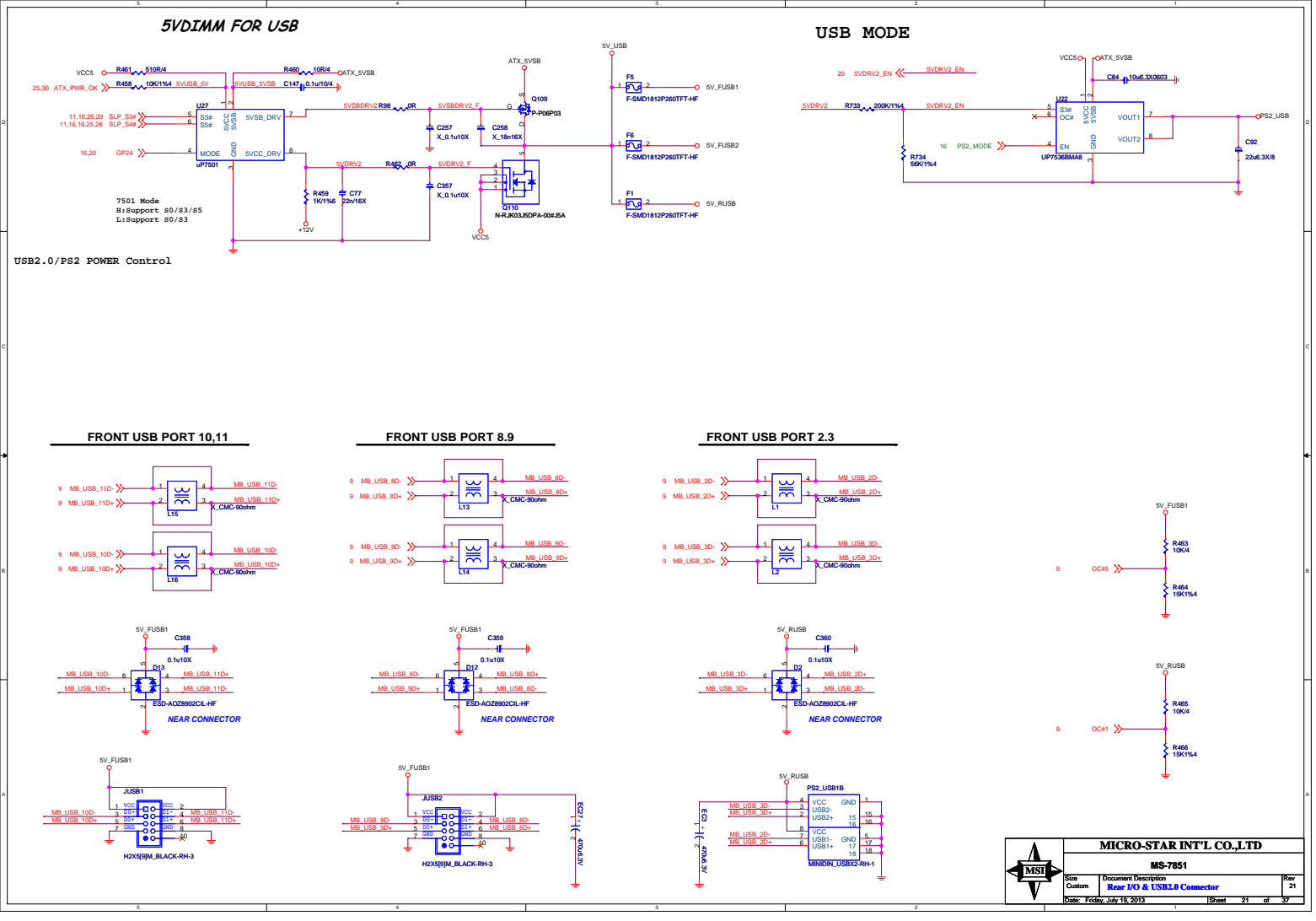
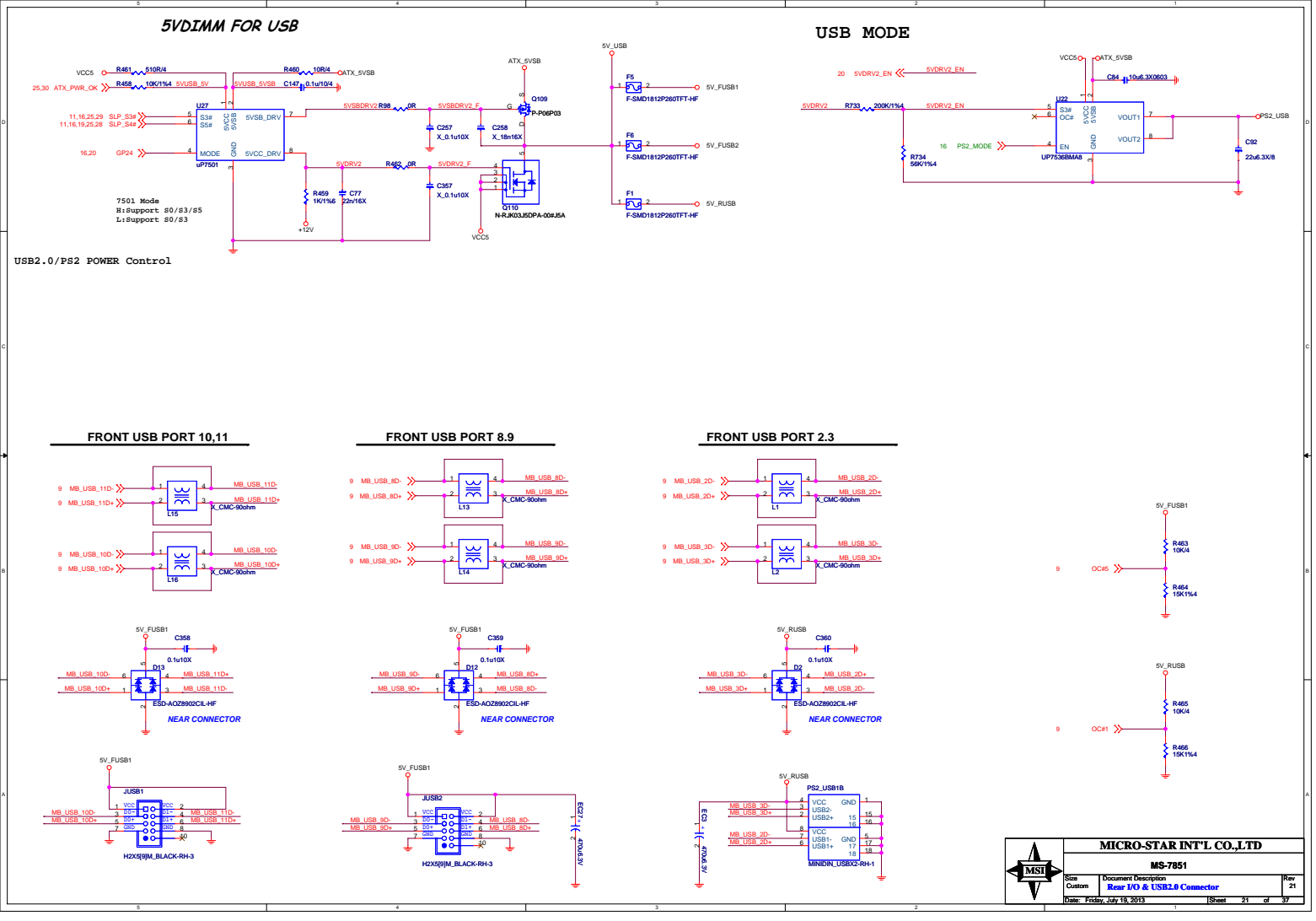
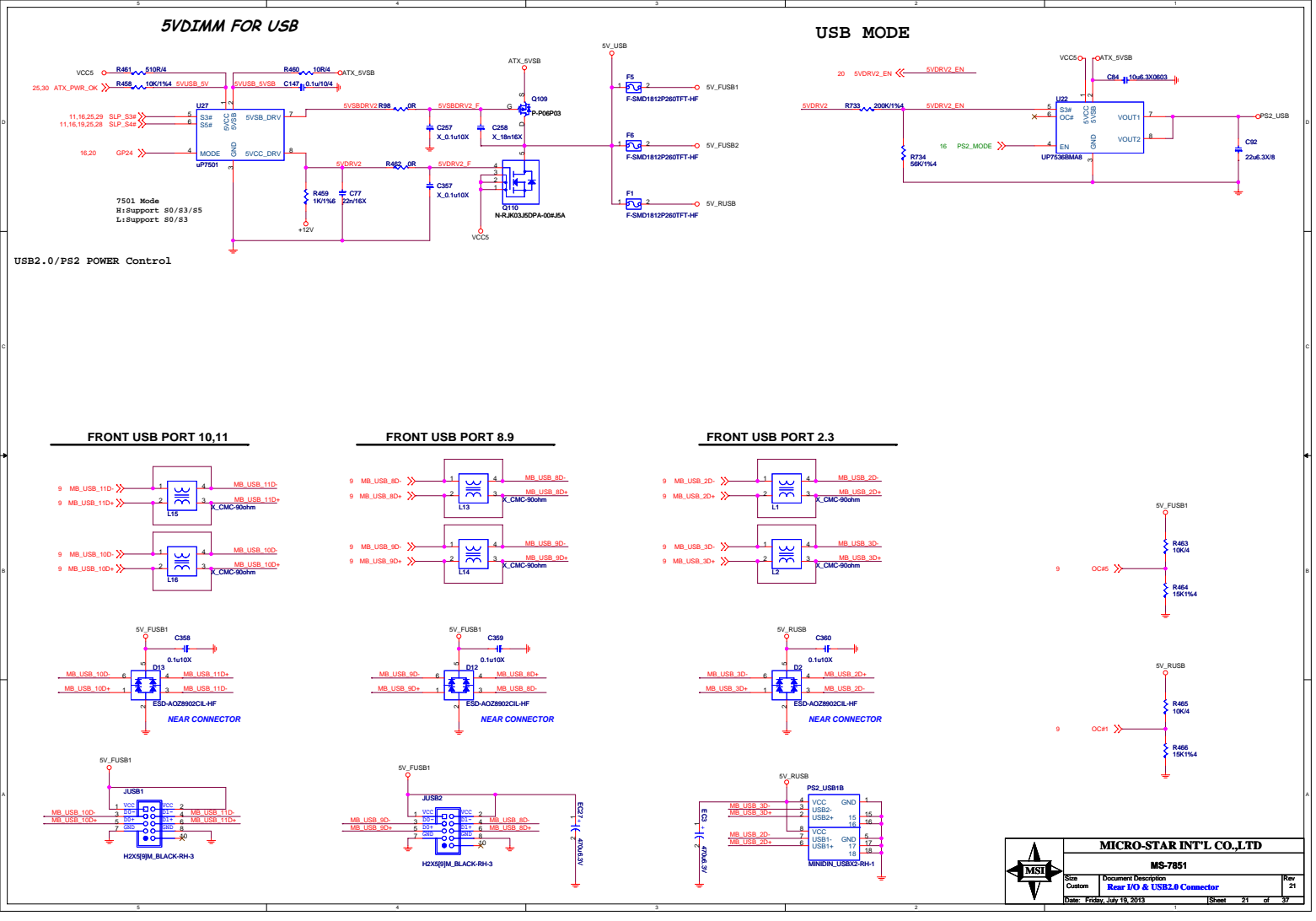
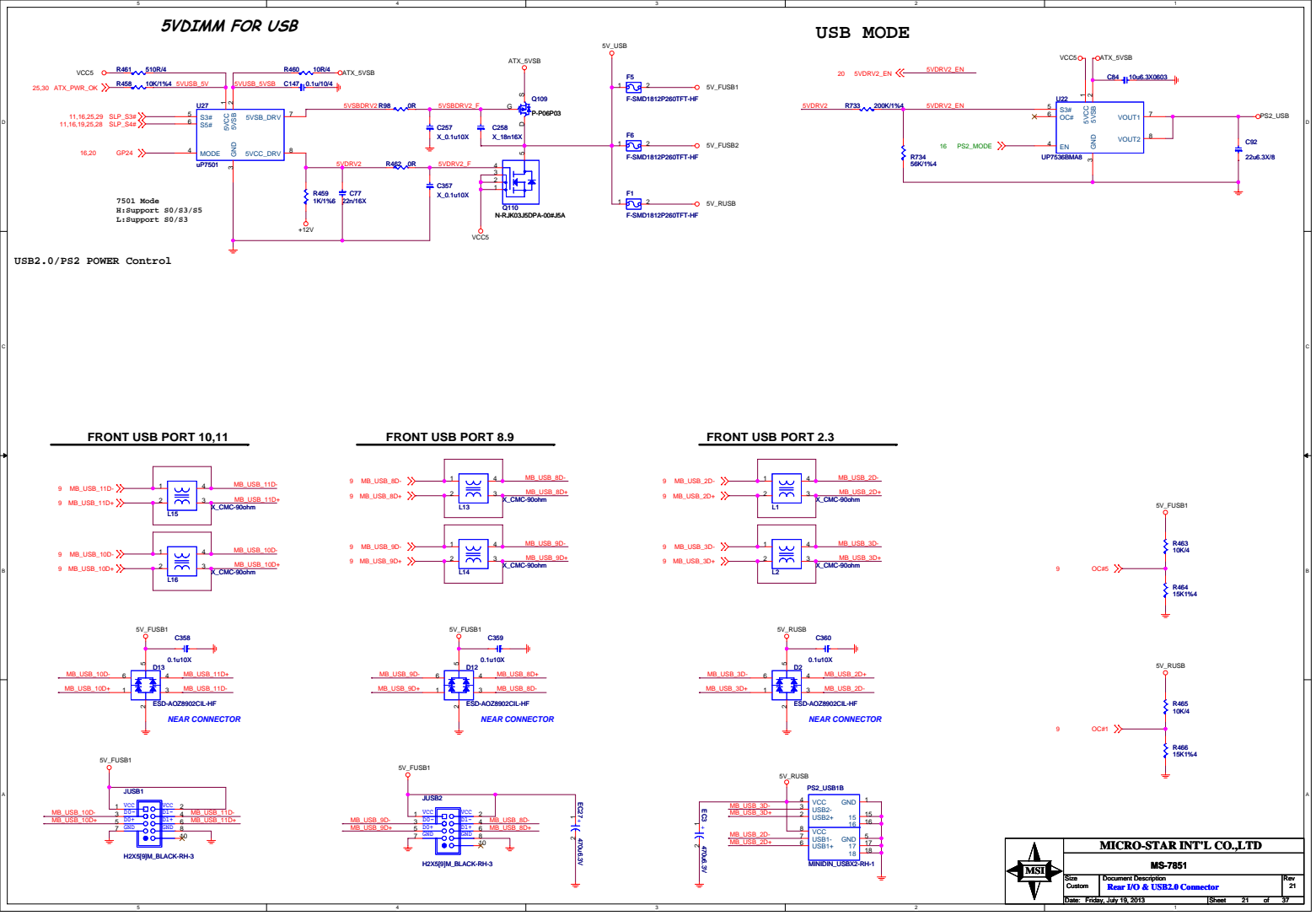
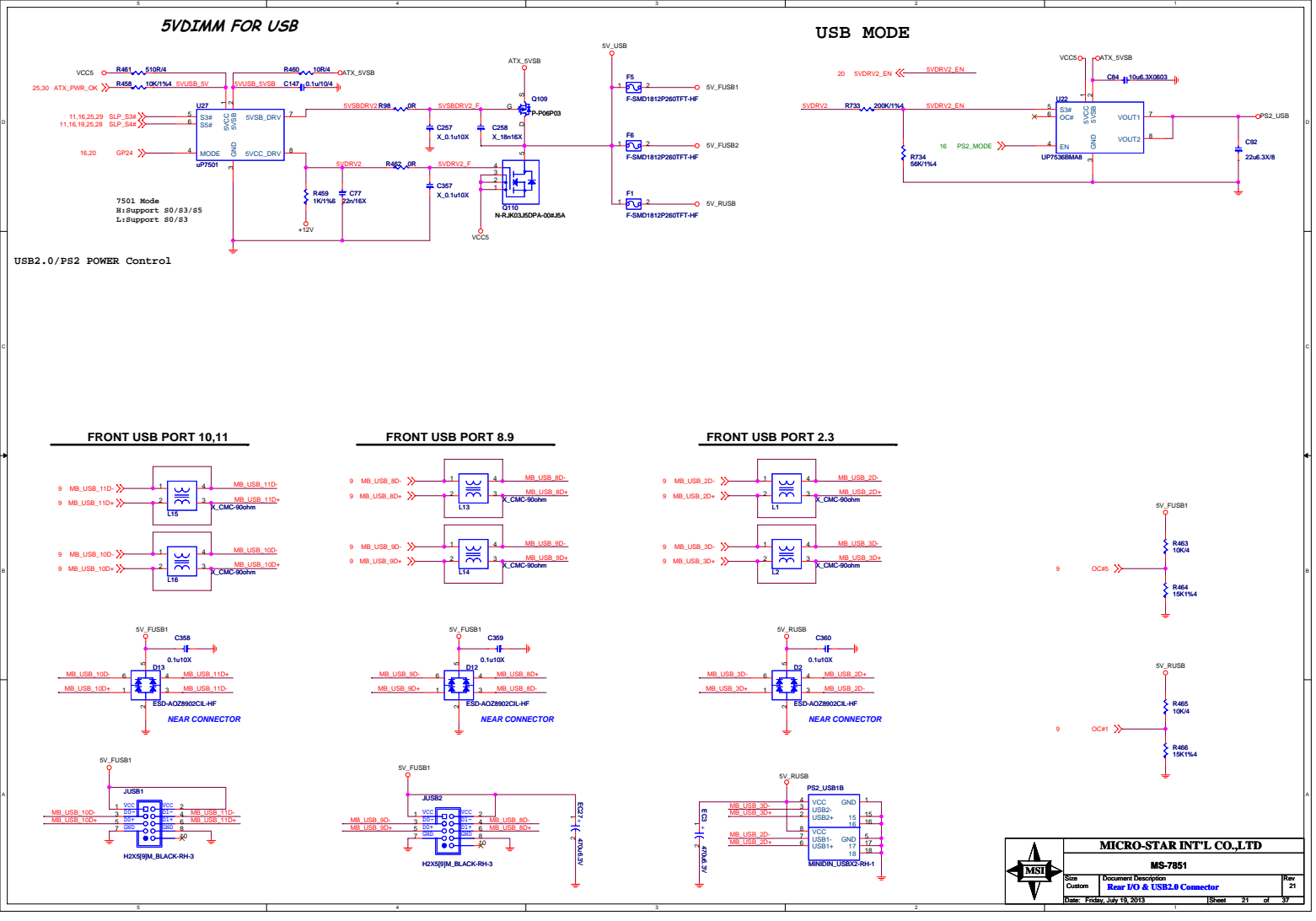
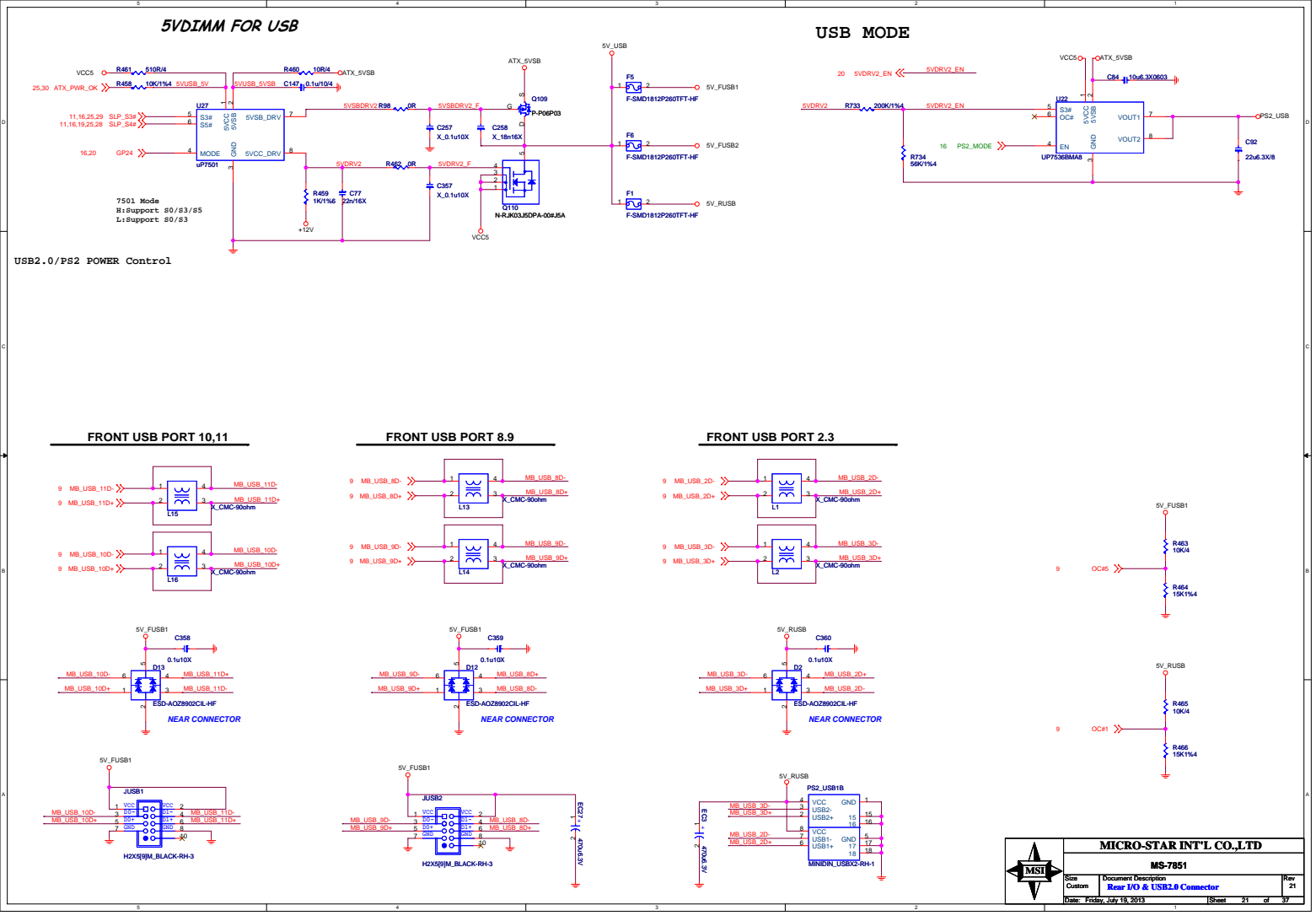
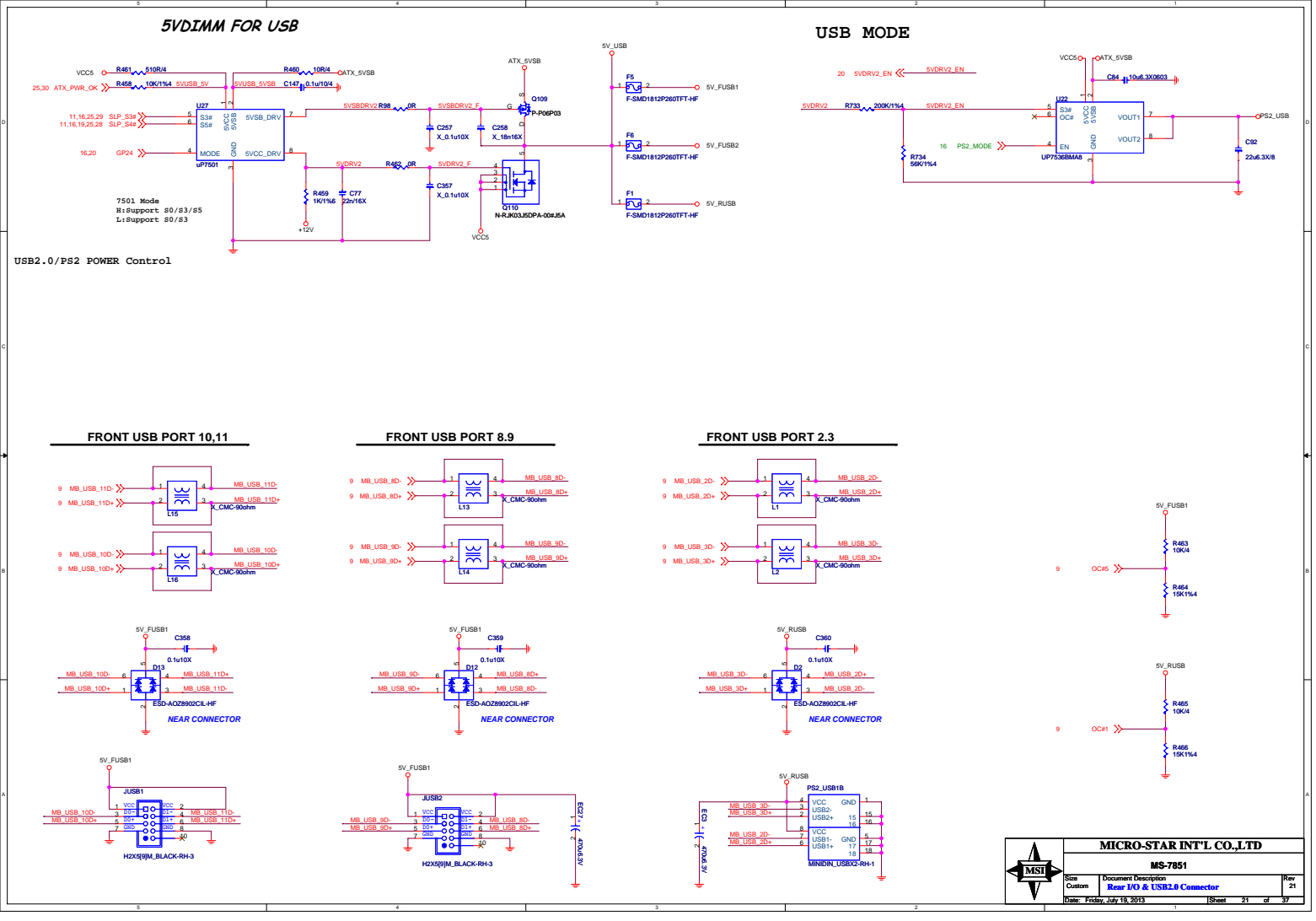
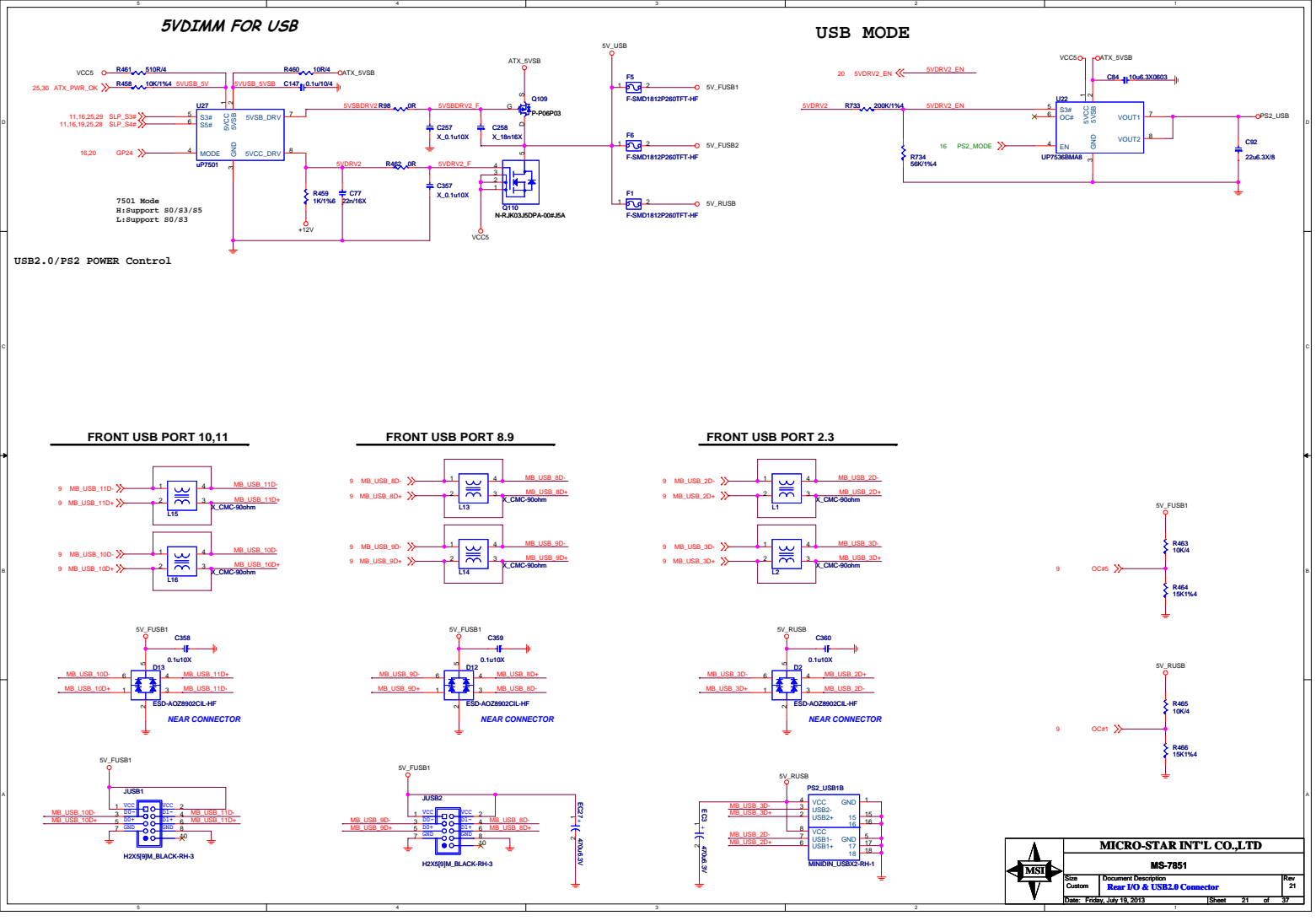
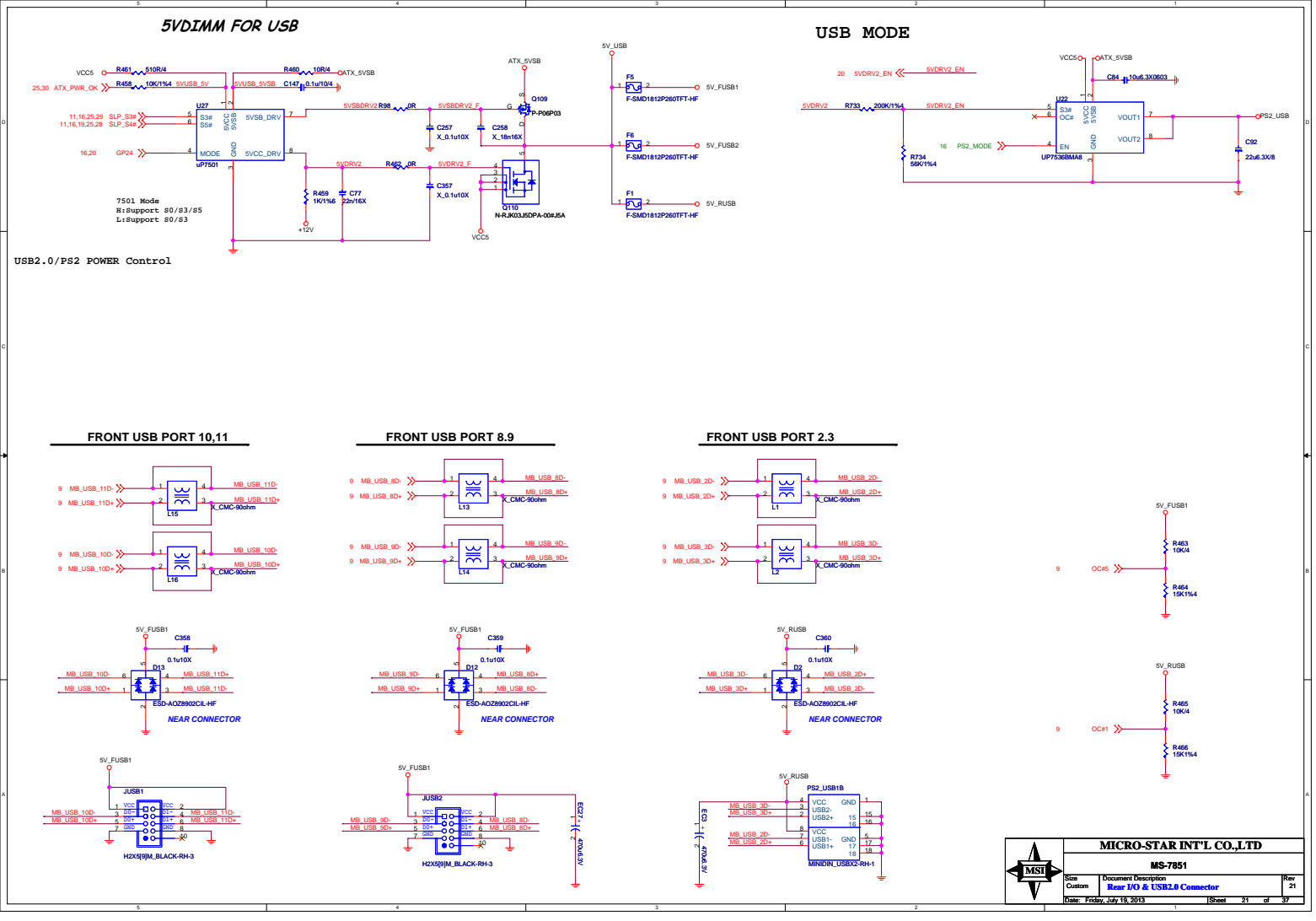
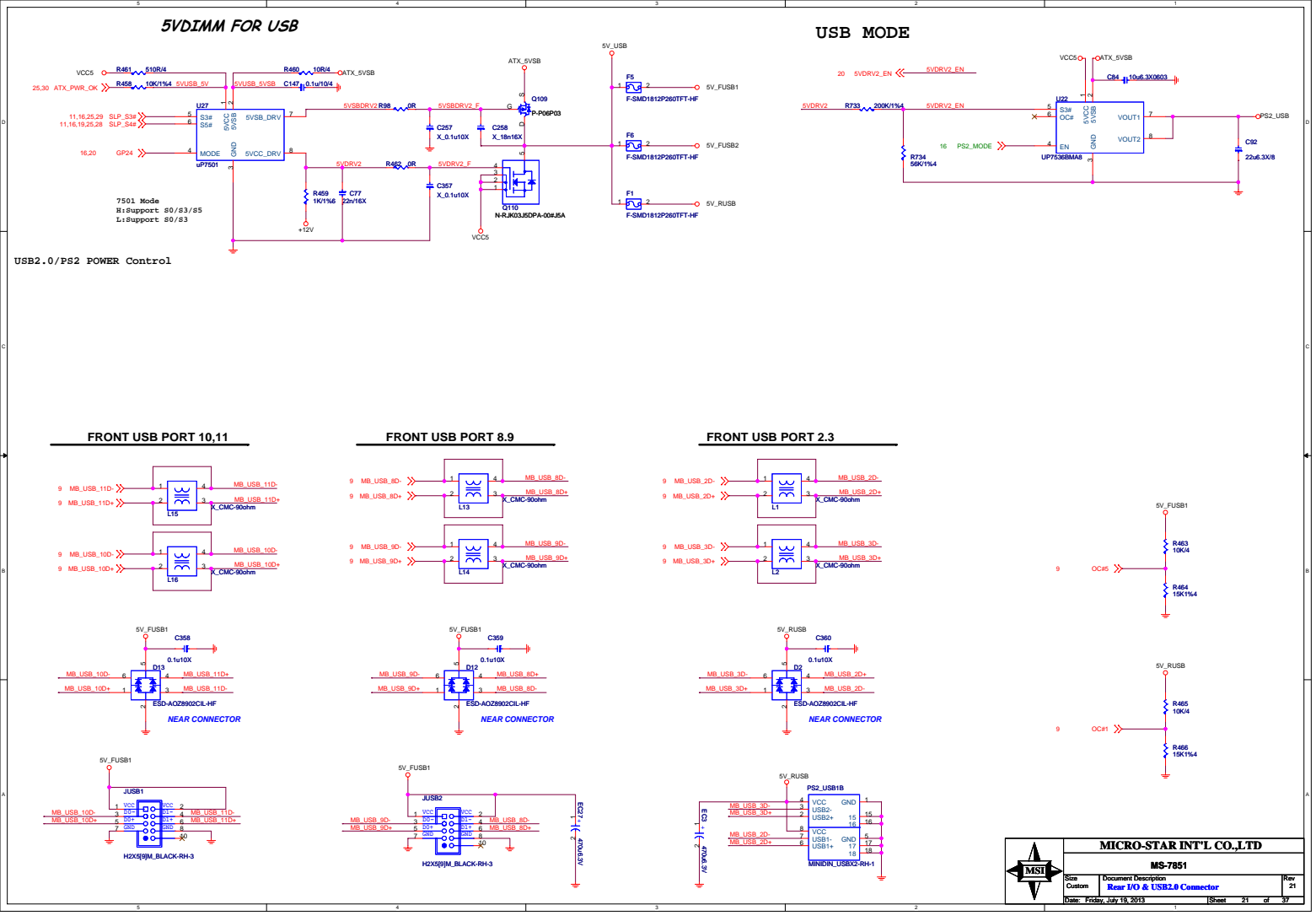
9 MB_USB_8D >> L13 MB_USB_8D-
9 MB_USB_8D+ >> MB_USB_8D+
X CMC-90ohm
9 MB_USB_9D >> L14 MB_USB_9D-
9 MB_USB_9D+ >> MB_USB_9D+
X CMC-90ohm
5V_FUSB1
C359 0.1uF10X
MB_USB_8D- 6
MB_USB_9D+ 3
MB_USB_8D+ 1
MB_USB_9D- 4
NEAR CONNECTOR
H2X59JM_BLACK-RH-3

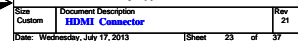
FRONT USB PORT 2,3

9 MB_USB_2D >> L1 MB_USB_2D-
9 MB_USB_2D+ >> MB_USB_2D+
X CMC-90ohm
9 MB_USB_3D >> L2 MB_USB_3D-
9 MB_USB_3D+ >> MB_USB_3D+
X CMC-90ohm
5V_FUSB1
C359 0.1uF10X
MB_USB_3D- 6
MB_USB_2D+ 3
MB_USB_3D+ 1
MB_USB_2D- 4
NEAR CONNECTOR
MINI-DIN_USB02-RH-1

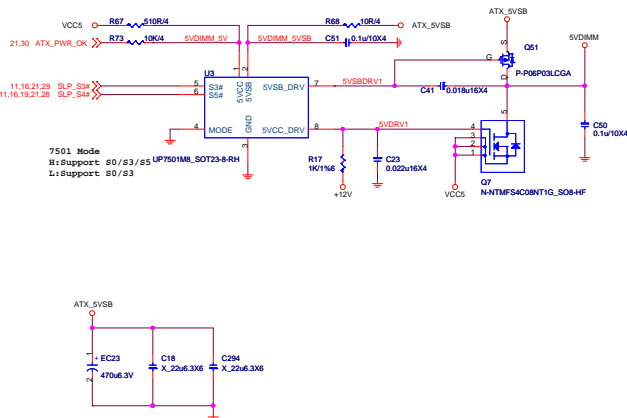
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Rear I/O & USB2.0 Connector
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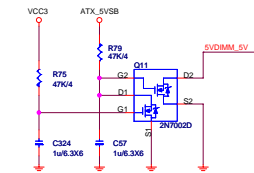
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5VDIMM FOR DDR



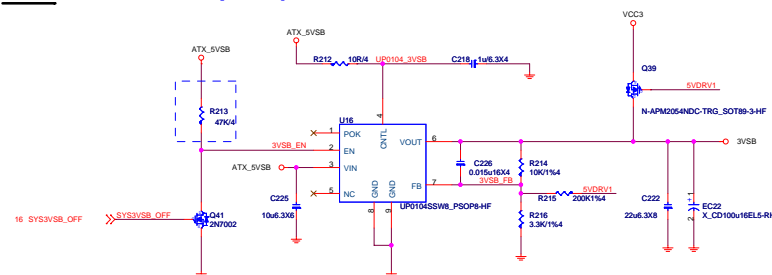
```
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.
```



Patch coolermaster 700w power sequence

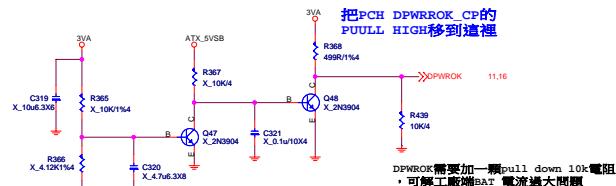
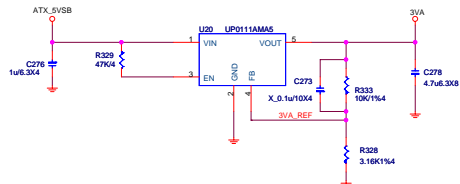
3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



3VA

20mA


$$\begin{aligned} 3.389\text{V分壓} &= 0.813\text{V} \\ 2.71\text{V分壓} &= 0.65\text{V} \end{aligned}$$

FOR DPWROK跟3VA的POWER
DOWN的時序(S5-->G3)

DPWROK需要加一顆pull down 10k電阻
，可解工廠端BAT 電流過大問題



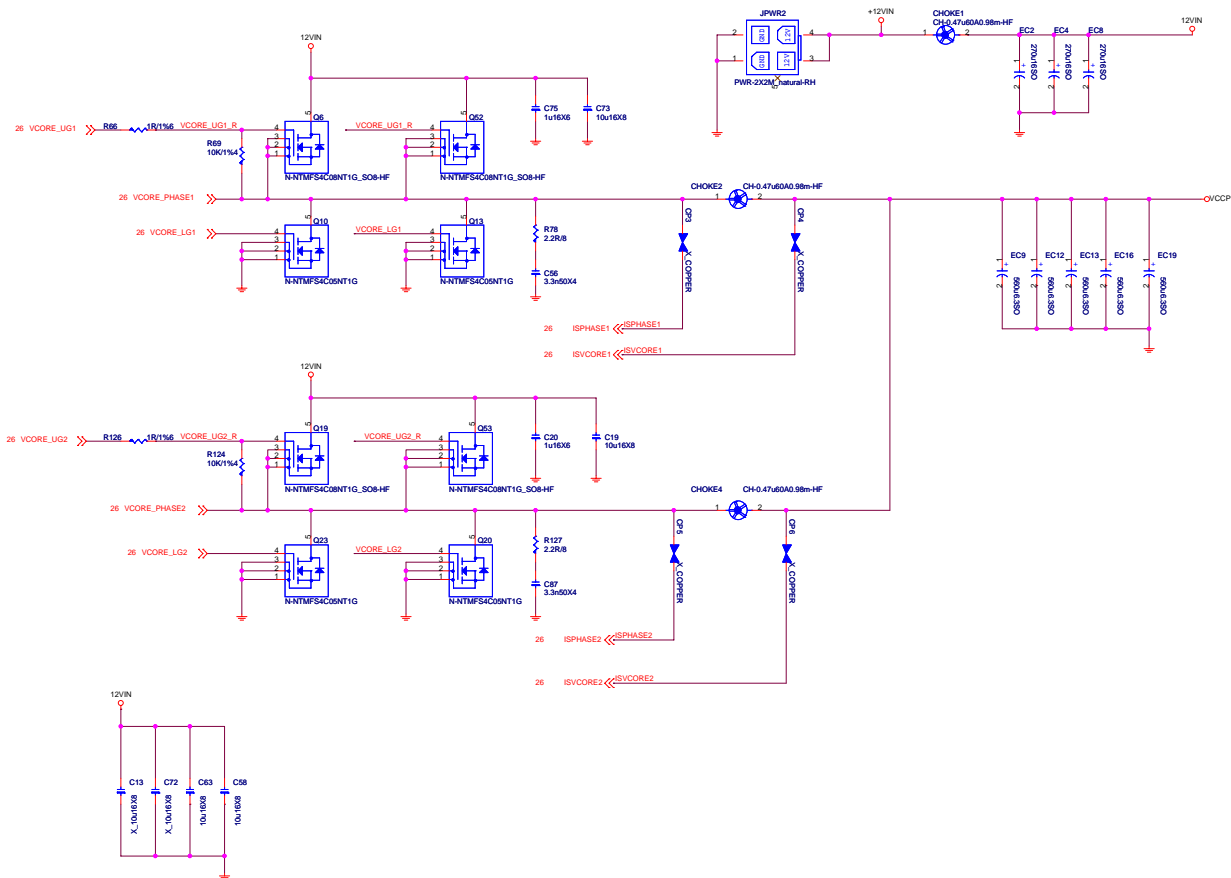
MICRO-STAR INT'L CO.,LTD

MS-7851

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VCCP POWER

VCORE ICC MAX70A ICCTDC:47A 65W
LL:2.5m ohm



OCP: 28A

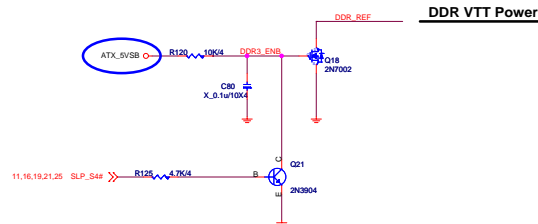
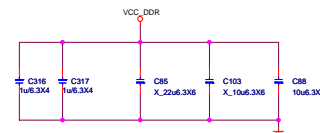
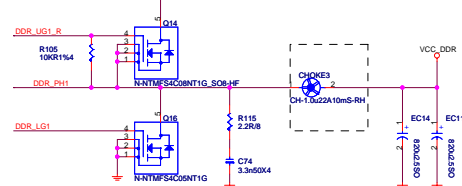
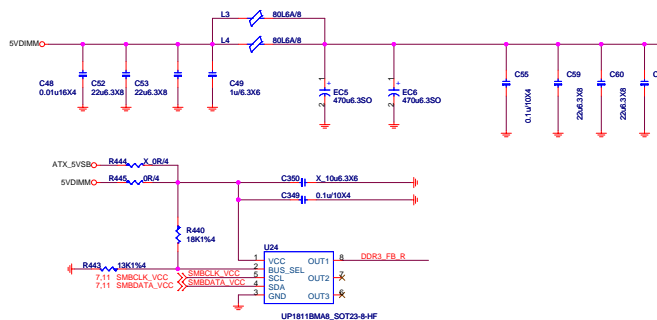
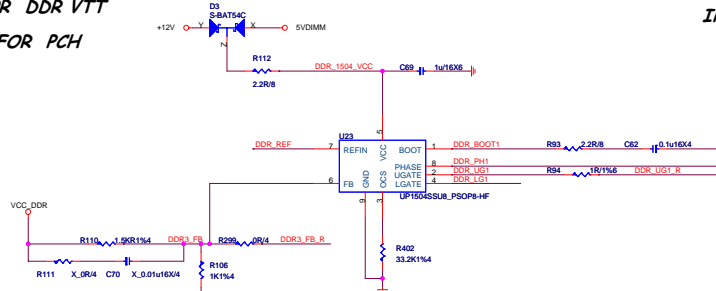
4.2A FOR CPU

6A FOR 2DIMM

0.5A FOR DDR VTT

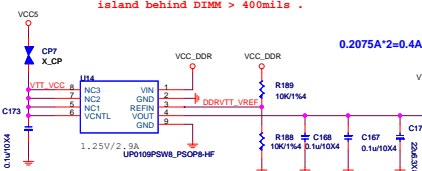
7.661A FOR PCH

OCP: 16.447*1.5=24.6705A

$$OCPXR_{dson}(Low\ side)=(40\mu A * R_{ocs}(R122))-0.4V$$
$$Rocs(R122)=13.75K$$
$$I_{inrush} = 18.361 * 1.5 / 5 / 0.8 = 6.9A$$


To CPU Copper trace width > 250mils , Fill
island behind DIMM > 400mils .

$$0.2075A \times 2 = 0.4A$$



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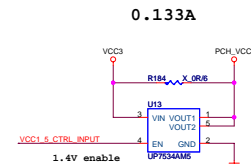
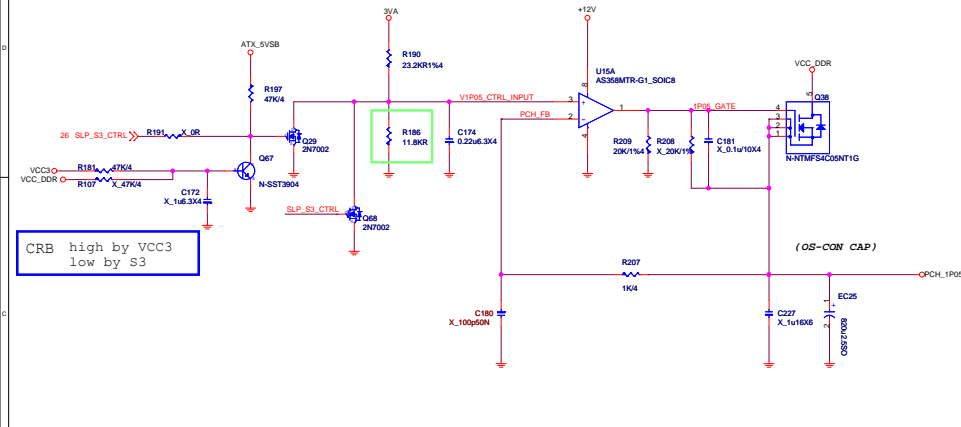
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Custom	DDR Power -UP1504S 1-Phase		
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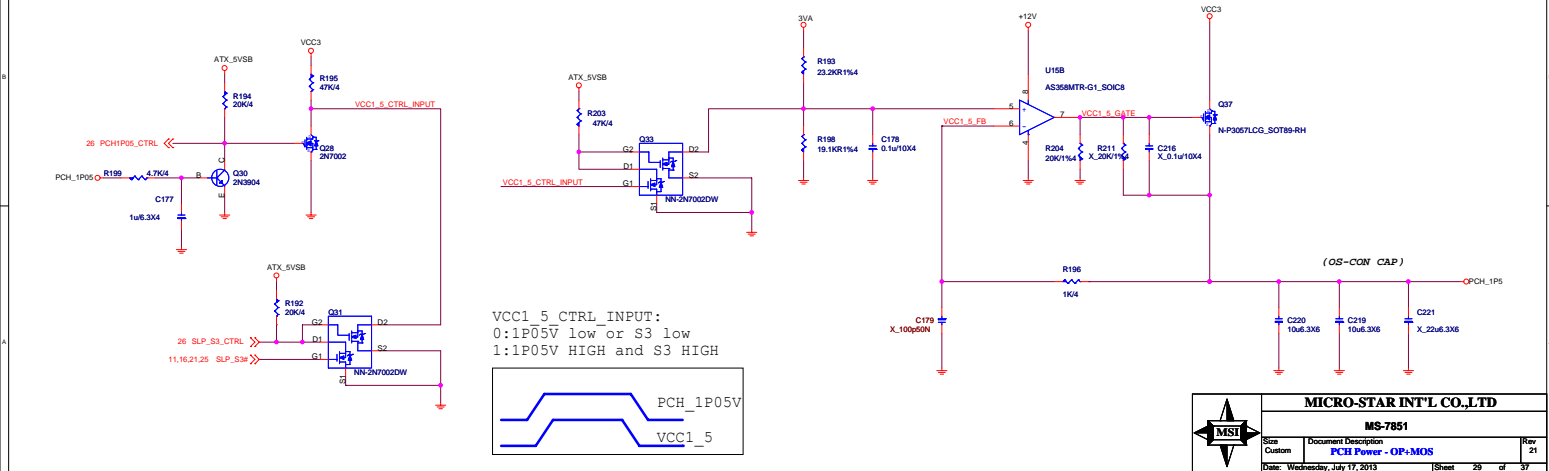
Date: Friday, July 26, 2013 Sheet 28 of 37

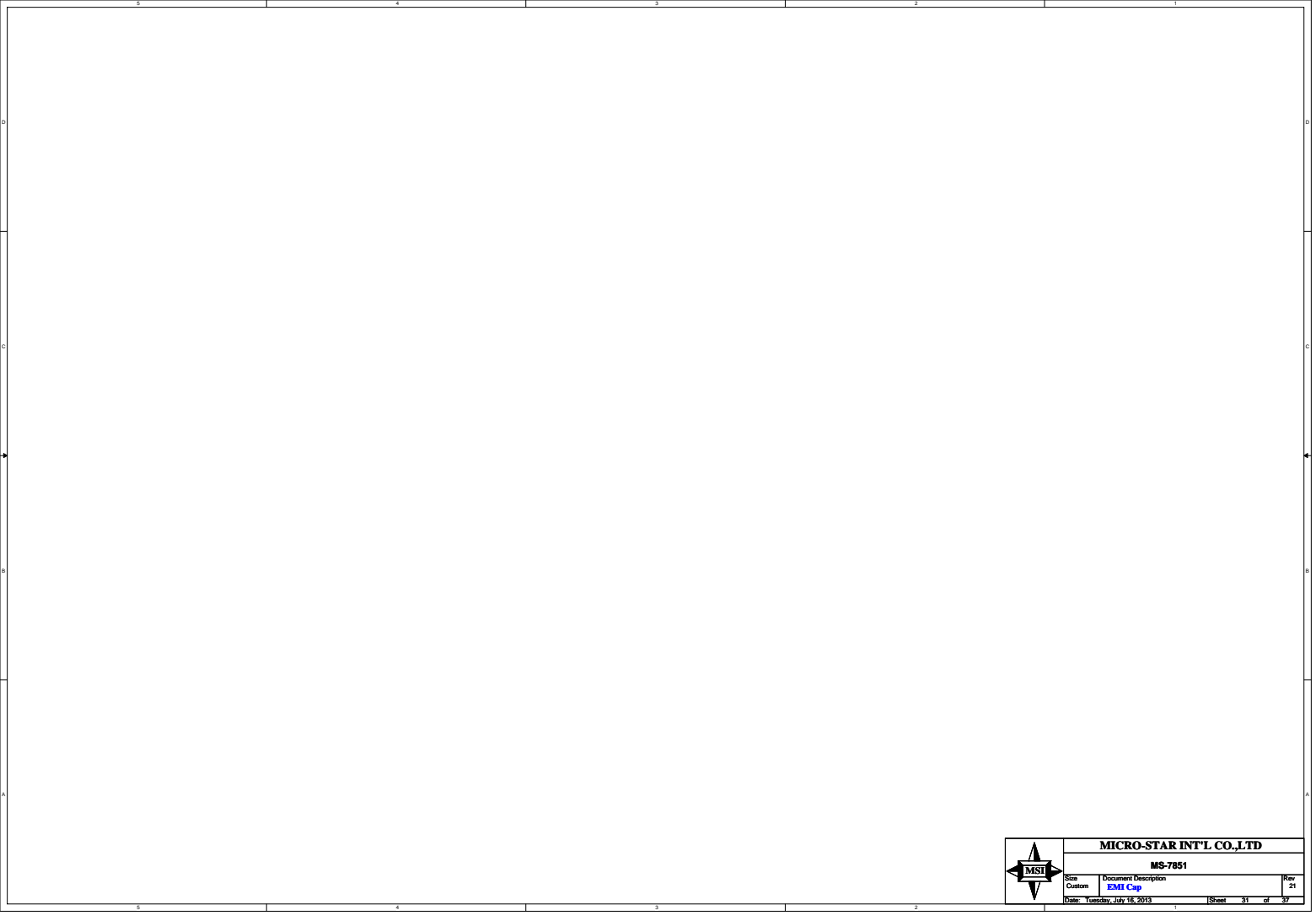
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PCH Power:1.05V 5.747A



PCH Power:1.5V 0.183A





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MS-7851		
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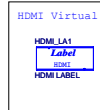
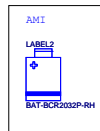
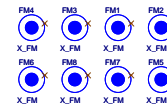
LABEL OPT.



LANUSB OPT.



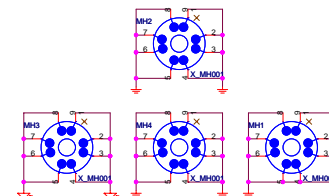
Optical Fiducial Marks-120



Simulation



Mounting Holes



PCH XDP PWRGD/RESET

